PATTERNING FOR ELONGATED V_{ss} CONTACT ON FLASH MEMORY

TECHNICAL FIELD

5   The present invention relates generally to the field of integrated circuit manufacture and, more particularly, to a method of improving the depth of focus and overlay margin within the stacked gate layer of a flash memory device.

BACKGROUND

10   Flash memory is a type of electronic memory media which can be rewritten and hold its content without power. Unlike dynamic random access memory (DRAM) and static random access memory (SRAM) memory chips, in which a single byte can be erased, flash memory is typically erased and written in fixed multi-bit blocks or sectors. Evolving out of electrically erasable read only

15 memory (EEPROM) chip technology, which can be erased in place, flash memory is less expensive and more dense. This new category of EEPROMs has emerged as an important non-volatile memory which combines the advantages of EPROM density with EEPROM electrical erasability.

      Conventional flash memories are constructed in a cell structure wherein a

20 single bit of information is stored in each cell. In such single bit memory architectures, each cell typically includes a metal oxide semiconductor (MOS) transistor structure having a source, a drain, and a channel in a substrate or P-well, as well as a stacked gate structure overlying the channel. The stacked gate may further include a thin gate dielectric layer (sometimes referred to as a tunnel

25 oxide) formed on the surface of the P-well. The stacked gate also includes a polysilicon floating gate overlying the tunnel oxide and an interpoly dielectric layer overlying the floating gate. The interpoly dielectric layer often is a multilayer insulator such as an oxide-nitride-oxide (ONO) layer having a nitride layer sandwiched between two oxide layers. Lastly, a polysilicon control gate overlies

30 the interpoly dielectric layer.

      Flash memory devices require a common source line, for example, to provide a connection to ground voltage (e.g., a V_{ss} contact) during a read operation. Generally, the V_{ss} contact is formed between stacked gate layers of

the flash memory device. As is known in the art, contacts are among the most difficult features to pattern in semiconductor manufacturing. Not only are they smaller than any other circuit structure (except gates), but their images are intrinsically 3-dimensional, with the same contact having minimum feature size in both x and y direction and the laws of diffraction reducing the range of focus along the z-direction.

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In a conventional method of forming the V_{ss} contact in a flash memory device, a gate oxide layer, a floating gate polysilicon layer, an inter-gate insulating layer and a control gate polysilicon layer are sequentially formed on a semiconductor substrate. Through photolithographic processes, the stacked layers are patterned to form a stacked gate pattern, e.g., a series of stacked gate layers. Impurities are implanted into the substrate using the stacked gate pattern as an implanting mask to form source/drain regions outside of the stacked gate pattern, and an interlayer insulating layer is deposited on the resulting structure. Using a photoetching process, the interlayer insulating layer is patterned between stacked gate layers to form a circular contact hole, exposing a predetermined region of the semiconductor substrate. A conductive layer is then deposited in the contact hole and on the interlayer insulating layer. A planarization process such as an etch-back or a chemical mechanical polish is carried out to leave the conductive layer in the contact hole and remove the portion of the conductive layer that is outside of the contact hole, thereby forming the V_{ss} contact.

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Referring to Fig. 1, a stacked gate pattern 10 of a prior art flash memory device is illustrated. A V_{ss} contact 12 is patterned between a first stacked gate layer 14 and a second stacked gate layer 16. As stated previously, the V_{ss} contact 12 typically is circular in shape.

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A pervasive trend in modern integrated circuit manufacture is to produce semiconductor devices, such as flash memory devices, that are as small as possible. The reduction in size of flash memory devices requires high resolution technology and a sufficient depth of focus (DOF), particularly in the formation of contact holes. DOF is the range of lens-wafer distances over which line widths are maintained within specifications and resist profiles are adequate. As flash memory devices are reduced in size, each stacked gate layer 14, 16 of the

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stacked gate pattern 10 is formed closer to adjacent stacked gate layers, thus requiring a smaller V_{ss} contact 12. As the V_{ss} contact 12 is reduced in size, DOF margin becomes an issue in patterning the V_{ss} contact. In present integrated circuit fabrication, DOF is becoming so small that it is a concern as to whether optical wafer steppers are capable of maintaining the image in focus. This problem is evident in forming components having small feature size, such as contact holes.

Another concern in integrated circuit manufacture is the lateral positioning between layers comprising the integrated circuit, which is known as overlay. As feature sizes shrink, the overlay tolerances must become smaller in order to minimize the creation of defective devices. The reduction in size of the flash memory device requires the V_{ss} contact 12 and adjacent stacked gate layers 14, 16 to be in closer proximity to one another, thus creating overlay margin issues.

As a result, there exists a need in the art for a method of patterning a V_{ss} contact in a flash memory device that improves the DOF margin and the overlay margin within the stacked gate layer.

SUMMARY OF THE INVENTION

According to one aspect of the invention, the invention is directed to a method of processing an integrated circuit wafer to form a contact in a flash memory device. The method can include forming a plurality of stacked gate layers on a semiconductor substrate, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; depositing an interlayer insulating layer over the plurality of stacked gate layers; patterning a contact hole between a first stacked gate layer of the plurality of stacked gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact hole is an elongated shape; and depositing a conductive layer in the contact hole.

Another aspect of the invention relates to flash memory device, including a plurality of stacked gate layers, wherein each stacked gate layer extends in a predefined direction and is substantially parallel to other stacked gate layers; and a contact formed between a first stacked gate layer of the plurality of stacked

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gate layers and a second stacked gate layer of the plurality of stacked gate layers, wherein the contact is formed in an elongated shape.

Other aspects, features, and advantages of the invention will become apparent from the following detailed description. It should be understood, however, that the detailed description and specific examples, while indicating several embodiments of the present invention, are given by way of illustration only and various modifications may naturally be performed without deviating from the present invention.

BRIEF DESCRIPTION OF DRAWINGS

Fig. 1 is a schematic top view of a prior art V_{ss} contact formed between stacked gate layers of a flash memory device.

Fig. 2 is a schematic top view of a V_{ss} contact formed between stacked gate layers of a flash memory device in accordance with an embodiment of the present invention.

Fig. 3 is a flow diagram illustrating an exemplary embodiment of a method of processing a wafer in accordance with the present invention.

Fig. 4A is a sectional view of a semiconductor wafer at a certain point during processing of the wafer using the method in accordance with an embodiment of the present invention.

Fig. 4B is a top view of the semiconductor wafer of Fig. 4A during another point of the wafer processing.

Fig. 4C is a cross-section taken along the line 1–1 of Fig. 4B.

Fig. 4D is a sectional view of the semiconductor wafer during another point of the wafer processing.

Fig. 4E is a top view of the semiconductor wafer of Fig. 4A during yet another point of the wafer processing.

Fig. 4F is a cross-section taken along the line 2–2 of Fig. 4E.

Fig. 4G is a sectional view of the semiconductor wafer during yet another point of the wafer processing.

Fig. 4H is a sectional view of the semiconductor wafer during yet another point of the wafer processing.

Fig. 5 is a schematic top view of a V_{ss} contact formed between stacked gate layers of a flash memory device in accordance with another embodiment of the present invention.

DISCLOSURE OF INVENTION

5   In the detailed description that follows, corresponding components have been given the same reference numerals, regardless of whether they are shown in different embodiments of the present invention or at difference times during a wafer processing method. To illustrate the present invention in a clear and

10   concise manner, the drawings may not necessarily be to scale.

Referring to Fig. 2, a stacked gate pattern 50 of a flash memory device in accordance with an embodiment of the invention is illustrated. The stacked gate pattern 50 includes a plurality of stacked gate layers 54, 56. As can bee seen in Fig. 2, the stacked gates layers 54, 56 of the stacked gate pattern 50 form a

15   series of rows, and the rows are substantially parallel to each other.

To assist in describing the invention, the stacked gates layers 54, 56 can be described with respect to a 3-dimensional Cartesian coordinate system. With respect to Fig. 2, for example, the z-axis is represented as the horizontal component (e.g., left to right), the y-axis is represented as the vertical

20   component (e.g., bottom to top), and the x-axis is represented as the depth component (e.g., coming out of the page). Thus, the "rows" of stacked gate layers lie in the z-axis, e.g., they form a line that extends along the z-axis, while the width and height components of each stacked gate layer lie in the y-axis and the x-axis respectively.

25   A V_{ss} contact 52 is formed between the first stacked gate layer 54 and the second stacked gate layer 56. The V_{ss} contact is formed in an elongated shape, such as an ellipse, for example, wherein a major axis 58 of the ellipse (i.e., the axis that passes through the foci of the ellipse) is substantially parallel to the stacked gate layers 54, 56, and the minor axis 60 of the ellipse (i.e. the axis

30   perpendicular to the major axis at the midpoint between the foci) is substantially perpendicular to the stacked gate layers 54, 56.

Since the major axis 58 of the ellipse is substantially parallel to the rows of stacked gate layers 54, 56 and the rows of stacked gate layers lie in the z-axis, it follows that the major axis 58 of the ellipse also lies in the z-axis. In light of the above and with reference to Fig. 2, it follows that the minor axis 60 of the ellipse lies in the y-axis. As will be explained in more detail below, the elongated shape provides a contact pattern that minimizes DOF and overlay issues during the fabrication of a flash memory device.

Eccentricity is a numerical value that determines the shape of an ellipse and is defined as the ratio of the distance between the foci to the length of the major axis. Eccentricity is always less than 1, and is expressed by the equation

$$\frac{\sqrt{(a^2 - b^2)}}{a} \qquad \text{Eq. 1}$$

where "a" is one half the length of the ellipse's major axis, and "b" is one half the length of the ellipse's minor axis. A perfectly circular ellipse has an eccentricity of 0, while an extremely long and narrow ellipse has an eccentricity that approaches 1. Thus, an elliptical contact having an eccentricity greater than zero, by definition, is not a perfect circle. Such an elliptical contact has a long or wide portion (the major axis) and a narrow or thin portion (the minor axis).

As packing densities of flash memory devices increase, the separation 62 between stacked gate layers is reduced. By forming an elliptical V_{ss} contact between stacked gate layers with its minor axis 60 substantially perpendicular to the stacked gate layers 54, 56, the length "b" of the minor axis 60 is constrained by one half of the separation 62 between stacked gate layers, plus any required overlay margin. This same constraint is imposed on prior art circular V_{ss} contacts, wherein a radius "r" of the circular contact must fit within the same limitations.

Thus, as the distance of separation 62 between stacked gate layers 54, 56 is reduced, the radius "r" of the circular V_{ss} contact and the minor axis "b" of the elliptical V_{ss} contact also must be reduced. A reduction in the radius of the circular V_{ss} contact has the effect of reducing the size of the circular V_{ss} contact in all directions since, by definition, a circle is composed of all points having a

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distance "r" from a center point. As the radius is reduced, the entire circle is reduced.

The elliptical V_{ss} contact 52, on the other hand, only is reduced along the minor axis 60. The major axis 58 is not affected by the reduction in separation

5   between stacked gate layers 54, 56. Therefore, the elliptical V_{ss} contact 52 formed between stacked gate layers 54, 56 can occupy a larger area than a circular V_{ss} contact formed between the same stacked gate layers. Moreover, the elliptical V_{ss} contact can be dimensioned along its major axis 58 so as to maintain feature size above a threshold value, and thus minimize DOF issues.

10   For example, the length of the major axis 58 can be increased as the length of the minor axis 60 is decreased, thereby maintaining the contact area above a threshold value.

Furthermore, since the elliptical V_{ss} contact 52 can overcome DOF issues by maintaining feature size above a threshold value (e.g., by increasing the major

15   axis 58), the minor axis 60 can be reduced to a greater extent than can the radius "r" of a circular contact. This provides an increase in overlay margin between the V_{ss} contact 52 and the stacked gate layers 54, 56 when compared to a circular V_{ss} contact. In one embodiment, the ratio of the minor axis length "b" relative to the major axis length "a" (e.g., a/b) is about 1.1 to 1.4, or in other words, the

20   length of the minor axis is about 71 percent to about 90 percent of the length of the major axis.

Referring to the flowchart 200 of Fig. 3 in conjunction with the diagrams of Fig. 4A - Fig. 4H, exemplary processing steps for fabricating the V_{ss} contact 52 between stacked gate layers 54, 56 of a flash memory device are shown.

25   The process begins with a layer of semiconductor material 100 as shown in step 202. In step 204, a gate oxide layer 102 is deposited or grown on a semiconductor substrate 100. Deposition or growth may be performed through various well known processes, such as chemical vapor deposition (CVD) or dry oxidation in an oxygen and nitrogen ambient atmosphere, for example. Following

30   the formation of the gate oxide layer 102, a floating gate layer 104 is deposited over the gate oxide layer in step 206, and in step 208 an inter-gate dielectric layer 106 is deposited over the floating gate layer 104. The inter-gate dielectric layer

106 typically is an oxide-nitride-oxide (ONO) composition and is formed using conventional techniques. For example, the ONO layer can be formed in a three-stage process, which includes forming a first film of silicon dioxide, depositing a film of silicon nitride on the silicon dioxide, and then depositing a

5   second film of silicon dioxide on the silicon nitride film.

At step 210, a control gate layer 108 is formed over the inter-gate dielectric layer 106. Formation of the control gate layer 108 includes, for example, depositing a layer of polysilicon material on the surface of the inter-gate dielectric layer 106 using low pressure chemical vapor deposition as is known by those

10   skilled in the art. Using conventional photolithographic processes, the stacked gate layer is patterned at step 212 to form a stacked gate pattern, e.g., stacked gate layers 54, 56, as shown in Fig. 4B and Fig. 4C.

Next at step 214, impurities are implanted into the substrate 100 using the stacked gate pattern as an implanting mask to form source 110 and drain 112

15   regions outside the stacked gate pattern, as is conventional. At step 216, an interlayer insulating layer 114 is deposited on the resulting structure, as shown in Fig. 4D. The interlayer insulating layer 114, for example, can be formed by depositing a silicon oxide film on the stacked gate pattern by means of sputtering or CVD and subsequently polishing the silicon oxide film by chemical mechanical

20   polish (CMP). Alternatively, the interlayer insulating layer 114 may be a multilayer film such as a silicon nitride film, an SOG (spin on glass) film or a BPSG (boron phosphor silicate lass) film.

Moving to step 218, a V_{SS} contact hole 116 is patterned in the interlayer insulating layer 114 between stacked gate layers 54, 56 using conventional

25   photolithographic techniques, as shown in Fig. 4E and Fig. 4F. As disclosed previously, the V_{SS} contact hole 116 is patterned in an elliptical shape, wherein the minor axis 60 of the ellipse is substantially perpendicular to the stacked gate layers 54, 56 and the major axis 58 of the ellipse is substantially parallel to the stacked gate layers 54, 56.

30   At step 220, the contact hole 116 is filled with a suitable conductive material (e.g., a metal, a metal containing compound or a semiconductor). For example, a conductive layer 118 such as a doped polysilicon layer or a metal

polycide layer is deposited in the contact hole 116 and on the interlayer insulating layer 114 as shown in Fig. 4G. Moving to step 222, a planarization process such as an etch-back or a chemical mechanical polish is carried out to leave the conductive layer in the contact hole and remove the portion of the conductive layer that is outside of the contact hole, thereby forming the V_{ss} contact 52 as shown in Fig. 4H.

As one skilled in the art will appreciate, the exemplary method described herein can be modified. For example, certain steps can be omitted, certain steps can be carried out concurrently, and other steps can be added.

Referring now to Fig. 5, a stacked gate pattern 50' of a flash memory device in accordance with another embodiment of the invention is illustrated. The stacked gate pattern 50' includes a plurality of stacked gate layers 54, 56. A V_{ss} contact 52' is formed between the first stacked gate layer 54 and the second stacked gate layer 56. The V_{ss} contact is formed in the shape of a rectangle, wherein a first pair of sides 300 are longer than a second pair of sides 302. The first pair of sides 300 lie in the z-axis and are substantially parallel to the stacked gate layers 54, 56. The second pair of sides 302 lie in the y-axis and are substantially perpendicular to the stacked gate layers 54, 56. With respect to the rectangular V_{ss} contact 52', a major axis 58' is defined as an axis parallel to the first pair of sides 300 and intersecting a midpoint of the second pair of sides 302, and a minor axis 60' is defined as an axis parallel to the second pair of sides 302 and intersecting a midpoint of the first pair of sides 300.

As was described previously with respect to the elliptical V_{ss} contact 52, the rectangular V_{ss} contact 52' formed between stacked gate layers 54, 56 can occupy a larger area than a circular V_{ss} contact formed between the same stacked gate layers. Additionally, the rectangular V_{ss} contact 52' can be dimensioned along the z-axis so as to maintain feature size above a threshold value, and thus minimize DOF issues. For example, the length of the first pair of sides 300 can be increased as the length of the second pair of sides 302 are decreased, thereby maintaining the contact area above a threshold value.

Furthermore, since the first pair of sides 300 of the rectangular V_{ss} contact 52' can be increased to maintain feature size above a threshold value, the length

of the second pair of sides 302 can be reduced to a greater extent than can the radius "r" of a circular contact. This provides an increase in overlay margin between the V_{SS} contact 52' and the stacked gate layers 54, 56 when compared to a circular V_{SS} contact. In one embodiment, the ratio of the second pair of sides 302 relative to the first pair of sides 300 (first pair/second pair) is about 1.1 to 1.4, or in other words, the length of the second pair of sides 302 are about 71 percent to about 90 percent of the length of the first pair of sides 300.

Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications and equivalents coming within the spirit and terms of the claims appended hereto. For example, while the exemplary embodiment has been illustrated using a floating gate memory cell, it will be appreciated by those skilled in the art that the invention also may be applied to a flash memory device employing a silicon-oxide-nitride-oxide-silicon (SONOS) memory cell.